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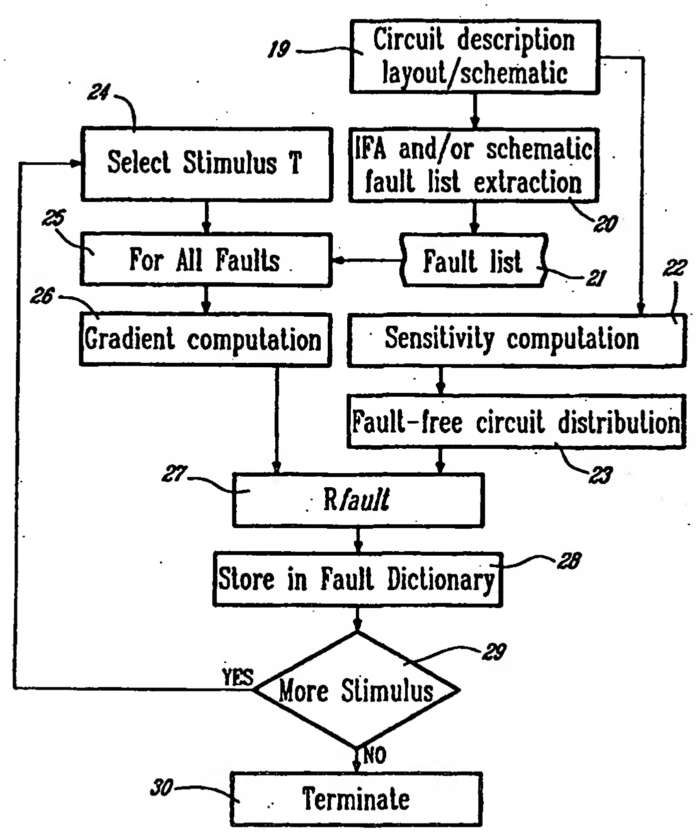
(54) Title: METHOD FOR PARALLEL ANALOG AND DIGITAL CIRCUIT FAULT SIMULATION AND TEST SET SPECIFICATION

(57) Abstract

In the method for constructing a fault dictionary, a description of the circuit is first made. A list of faults is extracted from this description of the circuit, and a fault-free circuit distribution of an output parameter of the circuit is calculated in response to the circuit description. A faulty circuit distribution of the output parameter is calculated in response to the faults of the list, and a fault value is calculated from the fault-free and faulty circuit distributions. The calculated fault value is stored in the fault dictionary in view of subsequently specifying a test vector for application to the circuit in view of testing this circuit. To specify test vectors in view of testing a given circuit, (a) a set of stimuli is first selected and then (b) a stimulus of this set is selected, (c) a fault from a list of faults of the circuit is selected, (d) a fault value related to the selected fault and stimulus is found in a fault dictionary, (e) the fault value found in step (d) is compared to a typical fault value, (f) whether the selected fault is detected or undetected by applying the selected stimulus to the circuit including the selected fault is determined in accordance with the result of the comparison of step (e), (g) steps (b, c, d, e and f) are repeated for each pair of stimulus and fault; and (h) test vectors are built from the stimuli of the set most susceptible to detect faults in the circuit.



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METHOD FOR PARALLEL ANALOG AND DIGITAL CIRCUIT FAULT SIMULATION AND TEST SET SPECIFICATION

BACKGROUND OF THE INVENTION

1. Field of the invention:

The present invention relates to a highly effective method for conducting parallel fault simulation and test set specification of digital and analog circuits. The method according to the invention formulates the fault simulation problem as a problem of estimating the fault value based on the distance between fault-free and faulty circuit distributions of the output parameter.

2. Brief description of the prior art:

Previous work in fault simulation and test generation focuses on digital circuits using the classical stuck-at fault model. Both serial and parallel fault simulation techniques have been developed. Algorithms for serial fault simulation constitute the simplest method of simulating faults. It consists of transforming the model of a fault-free circuit *N* to model a circuit *Nf* created by the fault *f*. Then *Nf* is simulated. The entire process is repeated for each fault of interest. Thus faults are

simulated one at a time [M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital Systems Testing and Testable Design", IEEE press, 1990]. Other fault simulation techniques, for example parallel, deductive, and concurrent fault simulation techniques have been developed and differ from the serial method in two fundamental aspects: a) they determine the behaviour of the circuit *N* in the presence of a fault without explicitly changing the model of the fault-free circuit *N* and, b) they are capable of simultaneously simulating a set of faults.

Research in the area of analog circuit fault simulation and test vector generation has not been as successful as its digital counterpart owing to the difficulty in modelling analog behaviour, the continuous nature of the analog input and output signals, the non-linearity of the circuit elements, and the complicated relation between the input and output signals referred to as "transfer function". Thus, because of the complex electrical nature of analog circuits, a direct application of the digital models has proved to be inadequate for capturing the faulty behaviour.

In the article of L. Milor and V. Visvanathan entitled "Detection of Catastrophic Faults in Analog Integrated Circuits", IEEE Trans. Computer-Aided Design, Vol. CAD-8, no.2, pp. 114-130, Feb. 1989, it has been suggested to model the faulty analog behaviour as a modification to the nominal macromodel. For instance, the fault model for a transistor has been implemented by replacing each transistor by a transistor surrounded by switches as shown in Figure 1. A faulty circuit can be obtained from the fault-free circuit by opening or closing the appropriate switch(es) 10, 11, 12 and/or 13.

In the article of R.J.A. Harvey, A.M.D. Richardson, E.M.J.G. Bruls, K. Baker, entitled "Analog Fault Simulation Based on Layout Dependent Fault Models", ITC 95, pp-641-649, to enable the circuit fault-effects to be simulated with a reasonable simulation time, behavioural models for each circuit block were developed. Hybrid fault simulations were performed by replacing each circuit block with its equivalent behavioural model to insert a target fault. Each fault is manually inserted in a netlist for simulation. The behavioural models reduced the simulation time by a factor of 10 to 36.

Hard fault modelling and simulation has been the subject of many publications:

- R.J.A. Harvey, A.M.D. Richardson, E.M.J.G. Bruls, K. Baker, "Analog Fault Simulation Based on Layout Dependent Fault Models", ITC 95, pp-641-649;

- L. Milor and V. Visvanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits", IEEE Trans. Computer-Aided Design, Vol. CAD-8, no.2, pp. 114-130, Feb. 1989;

- Naveena Nagi, A. Chatterjee, Jacob A. Abraham, "Fault Simulation Of Linear Analog Circuits", Analog Integrated Circuits and Signal Processing 1993;

- Majoj Sachdev, "A Realistic Defect Oriented Testability Methodology for Analog Circuits", JETTA 1993; and

- Naveena Nagi and Jacob A. Abraham, "Hierarchical Fault Modeling For Analog and Mixed-Signal Circuits", IEEE VLSI Test Symposium 1992, pp 92-101.

The presented approaches are all based on cause-effect analysis and do not enable parallel fault simulation. Indeed, cause-effect analysis enumerates all the possible faults (causes) existing in a fault model and determines all their corresponding responses (effects) to a given applied test in a serial manner. The required simulation time can become impractically long, especially for large analog designs.

OBJECTS OF THE INVENTION

An object of the present invention is to provide a method for performing parallel fault simulation and test vector specification based on effect-cause analysis. From the distance between a fault-free circuit distribution and a faulty circuit distribution (effect), the method according to the present invention approximate a fault (cause) value for all modelled faults simultaneously by linear estimation.

SUMMARY OF THE INVENTION

More specifically, in accordance with the present invention, there is provided a method for constructing a fault dictionary for

a circuit in view of subsequently testing the circuit, comprising the steps of:

(a) describing said circuit;

(b) extracting a list of faults from said description of the circuit;

(c) in response to the description of said circuit, calculating a fault-free circuit distribution of an output parameter of the circuit;

(d) calculating a faulty circuit distribution of the output parameter in response to the faults of said list;

(e) calculating a fault value from the fault-free and faulty circuit distributions;

(f) storing the calculated fault value in the fault dictionary in view of subsequently specifying at least one test vector for application to the circuit in view of testing said circuit.

The present invention also relates to a method for building test vectors in view of testing a given circuit, comprising the steps of:

(a) selecting a set of stimuli;

(b) selecting a stimulus of said set;

(c) selecting a fault from a list of faults of said circuit;

(d) from a fault dictionary, finding a fault value related to the selected fault and stimulus;

(e) comparing the faut value found in step (d) to a typical fault value;

(f) determining whether the selected fault is detected or undetected by applying said stimulus to the circuit including the selected fault in accordance with the result of the comparison of step (e);

(g) repeating steps (b), (c), (d), (e) and (f) for each pair of stimulus and fault; and

(g) building test vectors from the stimulus of said set most susceptible to detect faults in said circuit.

The objects, advantages and other features of the present invention will become more apparent upon reading of the following non restrictive description of a preferred embodiment thereof, given by way of example only with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the appended drawings:

Figure 1, which is labelled as "prior art" is a fault model for a transistor, consisting of a transistor surrounded by switches;

Figure 2 is a schematic view of an inverter layout, including an intermediate list of faults of this inverter layout, and a final list of faults obtained from the intermediate list after redundancies have been eliminated;

Figure 3 illustrates the circuit of a simple voltage divider;

Figure 4 is a complete list of 9 faults that can be found in the voltage divider of Figure 3;

Figure 5 is a reduced list of 6 faults built from the complete list of Figure 4 after removal of redundant and undetected faults;

Figure 6 is a graph showing examples of fault-free and faulty circuit distributions;

Figure 7 is a fault simulation flow chart as implemented by the method according to the invention for constructing a fault dictionary;

Figure 8 is a hard fault test vector specification algorithm;

Figure 9 is a schematic diagram of a second order band-pass filter;

Figure 10 is a list of 5 faults connected to the second order band-pass filter of Figure 9, indicating that 4 out of the 5 faults have been detected by means of a single test vector;

Figure 11 is a graph of the output parameter of the second order band-pass filter of Figure 9 versus the frequency of the test

vector, showing that for a test vector of 10 kHz the 4 detected faults of Figure 10 modified the output voltage (output parameter) by more than 5% with respect to the fault-free output voltage;

Figure 12 is a schematic diagram of the circuit of a fifth order chebychev filter; and

Figure 13 is a graph showing the fault coverage as a function of the number of test vectors for an inverter, a low pass filter, a state variable filter, a chebychev filter, a 4-bit analog-to-digital converter, an 8-bit analog-to-digital converter flash, and an 8-bit current digital-to-analog converter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fault simulation is used to construct a fault dictionary. Conceptually, a fault dictionary stores the signatures of faults in response to a specific stimulus T. Prior art fault simulation techniques are fault oriented and consists of:

(a) transforming a fault-free circuit N to a faulty circuit N*f* created by a fault *f* to simulate N*f* (the fault required by the fault-free circuit N to create the faulty circuit N*f* could be obtained from statistical analysis of circuit defects (Table 1));

(b) simulating the circuit in the presence of the fault *f*; and

(c) storing the signature (value of the output parameter) of each fault in the fault dictionary for use in test vector specification.

Constructing a fault dictionary through computation of every possible fault before testing is impractical.

TABLE 1 Upper and lower resistances used for hard fault modelling

Defect type	Lower Resistance (ohms)	Upper Resistance (ohms)
Added metal 1	0.2	1000
Added metal 2	0.2	1000
Via short	5	5
Junction leakage	100	10 000
Poly-metal 1 short	0.2	1000
Poly-metal 2 short	0.2	1000
Poly-poly short	20	1000
Open	1 Meg	∞

Figure 7 is a fault simulation flow chart, as implemented in the method according to the invention.

Step 19: A layout and/or schematic description of the circuit to be tested is first made.

Step 20: From the description of step 19, a layout-based fault list and/or a schematic-based fault list is/are extracted to form a fault list 21.

Step 22: The sensitivities of the output parameter to variations of circuit components due to manufacturing process variation is computed from the circuit description of step 19. The sensitivity is defined as the ratio of the relative deviation of the output parameter to the relative deviation of the circuit component.

Step 23: In step 23, the fault-free circuit distribution (see Figure 6) of the output parameter is computed in response to the circuit description (step 19) and the computed sensitivity (step 22).

Step 24: A stimulus T is selected.

Steps 25-26: The gradients of the output parameter with respect to all faults (step 25) are computed for the selected stimulus T (step 24). The output of step 26 is representative of the faulty circuit distribution (see Figure 6) of the output parameter in response to stimulus T.

Step 27: The fault value R_{fault} is calculated from the gradients computed in step 26 and the fault-free circuit distribution computed in step 23.

Step 28: R_{fault} calculated in step 27 is stored in the fault dictionary to form this fault dictionary.

Step 29: If the response to additional stimuli is desired, the algorithm returns to step 24.

Step 30: If no additional stimulus response is desired (step 29) the algorithm terminates.

Several steps of the algorithm of Figure 7 will be more clearly described hereinafter.

In accordance with the present invention, the fault dictionary is not constructed by storing the output signature of the fault *f* (effect), but by computing and storing the value R_{fault} of the fault (cause) by parallel fault simulation. For instance, R_{fault} indicates the value of the resistance that, if added to the circuit, will drive the output parameter under test out of a predetermined tolerance range. The output parameter is defined as a measured performance; the output parameter may be a voltage amplitude, a current amplitude or any other circuit response or specification. The fault list is first extracted and the fault value R_{fault} associated to the selected stimulus is then simultaneously calculated for all faults of the list from the fault-free and faulty circuit distributions of the output parameter, and stored in the fault dictionary. As will be explained in the following description, fault coverage and test vector specification can also be performed.

Steps 20 and 21:

The method according to the invention use a layout-based fault list and/or a schematic-based fault list. The layout-based fault list is used at macro level while the schematic-based fault list is used at a higher-level, i.e. at the level of interconnections between modules of the circuit. The schematic-based fault list is also used at early design stage where macro layouts are not available.

The method used to generate the layout-based fault list consists of moving a defect over the entire area of the layout. At each position taken by the defect, the polygons touch and their net numbers are obtained to deduce the fault produced by the defect [H. Wlaker and S.W. Director, "VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems", Vol. CAD5(4), pp 541-556, Oct. 1986]. When the defect has been moved over the entire layout, the layout-based fault list is complete. Each fault is described by its type , the coordinates of the defect responsible for the fault, and a probability related to the size of the responsible defect.

Example: A fault list was obtained for the inverter layout 14 of Figure 2. A total of 240 defects were inserted in the layout 14, which resulted in 26 faults. An intermediate faut list 15 gives the type of the fault and the coordinates (position) of the defect causing the fault. Eliminating the redundancy (step 17) led to the final fault list 16 of Figure 2, which contains three different

faults. In the final fault list 16, each fault is weighted by the number of occurrences.

Extraction of a schematic-based fault list is illustrated in Figures 3-5. The list shown in Figure 4 is not exhaustive since the only shorts listed are between the same element nodes. The method according to the invention also enables generation of all combinations of two, three or more shorted nodes. Using this feature may lead to a large list of faults containing a significant amount of nonrealistic faults. The example treated in Figures 3-5 does not include these combinations.

Example: In Figures 3-5, a simple voltage divider 18 (Figure 3) is taken as an example. The complete list of Figure 4 contains 9 faults. After having withdrawn the undetected and redundant faults from the complete list of Figure 4, the reduced list of Figure 5 containing 6 faults is obtained.

As an additional example, for a MOSFET transistor, the fault list is constructed of three shorts and two opens: short gate-source, short gate-drain, short source-drain, open drain, and open source.

Fault modelling and fault dictionary generation:

As indicated in the foregoing description, the present invention proposes to construct a fault dictionary by storing the fault value R_{fault} (*cause*) instead of storing the output parameter (*effect*). The effect is a constant value which represents the detectability threshold. The

cause is the minimal fault value that, if added to the circuit, will cause the output parameter to go out of a predetermined tolerance range and make the fault detectable. One way is to define the detectability threshold as (I) a constant absolute value deviation of the output parameter from its nominal value, for example $D_{threshold}$ = 10 *mv*, (ii) a constant percentage of the fault-free value of the output parameter, for example $D_{treshold}$ = 5%, or (iii) a constant factor of the fault-free circuit distribution of the output parameter and a constant factor of the faulty circuit distribution of the same output parameter, for example $3\sigma_{ff}$ and $3\sigma_{f}$, respectively.

The first two methods (i) and (ii) to define the detectability threshold are straightforward.

Steps 22 and 23:

For the third method (iii) (constant factors of the fault-free circuit distribution), a piecewise linear estimation is used to compute the fault-free circuit distribution of the output parameter due to process variations using Equation (1) [Naim B-Hamida, Khaled Saab, David Marche and Bozena Kaminska, "FaultMaxx: A Perturbation Based Fault Modeling and Simulation for Mixed-Signal Circuits", IEEE Asien Test Conference, October 1997; and Naim B. Hamida, Khaled Saab, David Marche, B. Kaminska and Gay Quesnel, "LIMSoft Automated Tool for Design and Test Integration of Analog Circuits", International Test Conference, 1996]. From Equation(1), the mean and standard deviation of the fault-free circuit output parameter can be obtained by means of Equations (2) and (3), respectively.

$$out = out_0 + \sum_{I-1}^{N} S_{x_I}^{out} \Delta x_I \qquad (1)$$

$$\mu_{out} = \mu_{out_0} + \sum_{I=1}^{N} S_{x_I}^{out} \mu_{\Delta x_I} \qquad (2)$$

$$\sigma_{out}^2 = \sum_{I=1}^{N} (S_{Y_I}^{out})^2 \sigma_{x_I}^2 + \sum_{I \neq j i=1}^{N} \sum_{j=1}^{N} S_{x_I}^{out} S_{x_j}^{out} \sigma_{x_{Ij}} \qquad (3)$$

where

- out_0 is the nominal value of the output parameter;
- *out* is the estimated value of the output parameter due to variation of the components;
- Δx_i is the variation of the circuit component x_i due to process variation;
- S_{xi}^{out} is the sensitivity of *out* to x_i;
- σ_{xi} is the standard deviation of the component x_i; and
- σ_{xij} are covariance terms.

Steps 24-26:

Now, if the faulty circuit distribution of the output parameter and its standard deviation due to added resistance are computed, equations (1), (2) and (3) respectively become

$$out = out_0 + \sum_{i=1}^{N} S_{x_i}^{out} \Delta x_i + G_{f_i}^{out} R_{f_i} \tag{4}$$

$$\mu_{out} = \mu_{out_o} + \sum_{i=1}^{N} S_{x_i}^{out} \mu_{\Delta x_i} + G_{f_i}^{out} \mu_{R_{f_i}} \tag{5}$$

$${}^{2}_{out} = \sum_{i=1}^{N} (S_{x_i}^{out})^2 \sigma_{x_i}^2 + \sum_{i \neq j i=1}^{N} \sum_{j=1}^{N} S_{x_i}^{out} S_{x_j}^{out} \sigma_{x_{ij}} + (G_{f_i}^{out})^2 \sigma_{R_{f_i}}^2 + \sum_{i=1 j=1}^{N} G_{f_j}^{out} S_{x_i}^{out} \sigma_{x_i R_{f_i}} \tag{6}$$

where R_{fi} is the newly added component due to short or open and G_{fi}^{out} is the gradient of *out* with respect to the fault f_i, σ_{Rfi} is the standard deviation of the fault value (resistance), and σ_{xiRfi} is the covariance term between the newly added component and the components in the original fault-free circuit.

Since σ_{Rfi} is always equal to zero, and if we consider the variable as independent, the covariance terms σ_{xiRfi} are equal to zero, the expression for the faulty output variance is greatly simplified, and Equation (6) reduces to

$$\sigma_{out}^2 = \sum_{i-1}^{N} (S_{x_i}^{out})^2\, \sigma_{x_i}^2 + \sum_{i\neq j\, i=1}^{N}\sum_{j=1}^{N} S_{x_i}^{out} S_{x_j}^{out} \sigma_{x_{ij}} \qquad (7)$$

Thus, under the above assumptions, hard defects do not modify the fault-free circuit standard deviation ($3\sigma_f = 3\sigma_{ff}$) but affect only the mean value.

Now that the fault-free and faulty circuit distributions of the output parameter are obtained, the detectability threshold is set to be the minimal distance between the fault-free and faulty circuits that guarantee detectability of the fault (Figure 6). This minimal distance is given by the relation:

$$D_{threshold} = \mu_f - \mu_{ff} \approx 3\sigma_f + 3\sigma_{ff} \qquad (8)$$

where μ_{ff} and μ_f are the mean output parameter values for the fault-free and faulty circuit distributions, respectively, and σ_{ff} and φ are the estimated fault-free and faulty output standard deviations of these distributions, respectively.

Step 27:

The fault value R_{fi} could now be obtained from Equations (2) and (5):

$$R_{f_i} \approx \frac{|\mu_f - \mu_{ff}|}{G_{f_i}^{out}} \approx \frac{|3\sigma_f + 3\sigma_{ff}|}{G_{f_i}^{out}} \tag{9}$$

$$R_{f_i} \approx \frac{6\sigma_{ff}}{G_{f_i}^{out}} \tag{10}$$

combining (3) and (10), we obtain

$$R_{f_i} = \frac{6\sqrt{\sum_{i=1}^{N}(S_{x_i}^{out})^2\sigma_{x_i}^2 + \sum_{i\neq j, i=j=1}^{N}\sum^{N} S_{x_i}^{out}\, S_{x_j}^{out}\sigma_{x_{ij}}}}{G_{f_i}^{out}} \tag{11}$$

where S and G (steps 22 and 26, respectively) are obtained using the well known adjoint network method [Stephan W. Director and Ronald A. Rohrer, "Automated Network Design - The Frequency Domain Case", IEEE Trans. on Circuit Theory, CT-16, no. 3, August 1969, pp 330-337; J. Chojcan and J. Izydorcky, "The Time domain Sensitivity computation Using SPICE2. The Linear Network Case", Proceedings Intern, AMSE conference "Signal & System", Cetinje (Yugoslavia), Sep. 3-5, 1990, Vol 3, pp 113-123; Leon O. Chua and Pen-Min Lin, "Computer-Aided Analysis of Electronic Circuits", Prentice-Hall, INC. "Englewood Cliffs, New Jersey, 1975; Stephan W. Director and Ronald A. Rohrer, "The Generalized

Adjoint Network and Network Sensitivities", IEEE Trans. on Circuit and Theory, Vol. CT-16, no. 3, August 1969, pp. 318-323; and Tellegen B.D.H., "A General Network Theorem, with Application", Phillips Res. Dept. no. 7, pp 259-269]. The adjoint network method allows to compute the sensitivities of one output parameter with respect to all component variations (existing and non-existing components) in only two simulations, one for the original network and one for the corresponding adjoint network. The adjoint network method for sensitivity computation in AC, DC and transient domain has been implemented using Hspice [Meta-Software, "HSPICE User's Manual version H92", Meta-Software, Inc. 1992] as a basic simulator [Naim B-Hamida, Khaled Saab, David Marche and Bozena Kaminska, "FaultMaxx: A Perturbation Based Fault Modeling and Simulation for Mixed-Signal Circuits", IEEE Asien Test Conference, October 1997; Saab Khaled, Naim B. Hamida, David Marche and Bozena Kaminska, "LIMSoft: Automated Tool for Sensitivity Analysis and Test Vector Generation", IEEE Proceedings on Circuits, Devices and Systems, December 1996; and Naim B. Hamida, Khaled, Saab, David Marche, B. Kaminska and Gay Quesnel, "LIMSoft Automated Tool for Design and Test Integration of Analog Circuits", International Test Conference, 1996].

Knowing the component tolerance Δx_i, the output parameter distribution of the fault-free and faulty circuit $3\sigma_{ff}$ and $3\sigma_f$ are estimated. Then equation (11) enables estimation of the resistance value R_{fault} that will cause the output parameter to go out of the tolerance range.

Step 28:

The values R_{fault} are stored in the fault dictionary.

In summary, from the fault-free circuit distribution, the mean value and standard deviation of the output parameter due to circuit component variations is computed. Then, from the fault-free circuit distribution of the output parameter and the gradient values calculated in step 26, the resistance value that will drive the output parameter out of its tolerance range is computed and stored. Note that the resistance value which is obtained indicates the value of the resistance which, if added to the branch or circuit, will cause the output parameter to go out of its tolerance range. This resistance value will be used for test vector specification.

The following section describes an algorithm which uses the fault dictionary generation approach and fault dominance concept to derive the fault coverage and the test vector specification that detect the largest set of faults without targeting individual faults.

Fault Dominance:

In digital circuits, fault dominance is used to reduce the number of faults that need to be considered.

Definition [M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital Systems Testing and Testable Design", IEEE press, 1990.]: Let T_g be the set of all tests that detects a fault g. Let's say that a fault f dominates a fault g if f and g are equivalent under T_g.

In other words, if f dominates g then any test that detects g, will also detect f (on the same primary output). Therefore, for

fault detection it is unnecessary to consider the dominating fault f, since by deriving a test to detect g we automatically obtain a test that detect f as well.

In analog circuit, the input/output relationship is more complex, but to the first order approximation, the above fault dominance theorem could be used as well.

Indeed, instead of testing for the upper and lower resistance values for faults as described in R.J.A. Harvey, A.M.D. Richardson, E.M.J.G. Bruls, K. Baker, "Analog Fault Simulation Based on Layout Dependent Fault Models", ITC 95, pp-641-649 (Table 1), in the present invention, fault dominance will be used where only the least dominating upper resistance will be tested for shorts, and the least dominating lower resistance will be tested for opens.

Test Vector Specification:

An example of hard fault test vector specification algorithm is illustrated in Figure 8.

Step 31: A set of stimuli is selected. A default stimulus could be used or it can be made by the test engineers in an interactive mode in order to consider any special characteristic of a circuit. Stimuli are divided into DC, AC and transient stimuli [Majoj Sachdev, "A Realistic Defect Oriented Testability Methodology for Analog

Circuits", JETTA 1993.]: sine wave, pulse, ramp, any PWL function, etc.

Step 32: A stimulus T is selected from the set of stimuli of step 31.

Step 33: A fault is selected from a fault list 48 constructed by the algorithm of Figure 7.

Step 34: Step 34 is responsive to the selected stimulus from step 32 and the fault selected in step 33 to obtain a value of R_{fault} from a fault dictionary 49.

Step 35: Step 35 determines whether the fault is an open or a short.

Steps 36-40: - If the fault is an open (step 35) and $R_{fault} < R_{typical}$ (step 36; Table 1 presents a list of circuit defects and the corresponding typical resistance range obtained by statistical analysis of circuit defects [R.J.A. Harvey, A.M.D. Richardson, E.M.J.G. Bruls, K. Baker, "Analog Fault Simulation Based on Layout Dependent Fault Models", ITC 95, pp-641-649], the fault is removed from the fault list (step 39) and the fault is marked as being detected by simulus T (step 40). Then, it is concluded that R_{fault} (or higher resistance value) will cause the output parameter to deviate out of tolerance and the simulus T is accepted as a valid test vector;

- if the fault is an open (step 35) and $R_{fault} > R_{typical}$ (step 36), the fault is marked as being undetected by simulus T (step 38). Then, it is concluded that no deviation of the output parameter could be detected and the stimulus T is rejected as a valid test vector;
- if the fault is a short (step 35) and $R_{fault} > R_{typical}$ (step 37), the fault is removed from the fault list (step 39) and the fault is marked as being detected by simulus T (step 40). Then, it is concluded that R_{fault} (or higher resistance value) will cause the output parameter to deviate out of tolerance and the simulus T is accepted as a valid test vector; and
- if the fault is a short (step 35) and $R_{fault} < R_{typical}$ (step 37), the fault is marked as being undetected by simulus T (step 38). Then, it is concluded that no deviation of the output parameter could be detected and the stimulus T is rejected as a valid test vector.

Step 41: In this step, the algorithm is returned to step 33 until all faults in the fault list have not been processed for a given stimulus T.

Step 42: In this step, the algorithm is returned to step 32 as long as all the stimuli of the set selected in step 31 have not been processed.

Step 43: The fault coverage is printed; this is a list of faults that can be detected by the set of stimuli selected in step 31.

Step 44: The test vectors are printed; this constitutes the test vector specification.

Step 45: The test algorithm is terminated.

Therefore, the fault values R_{fault} corresponding to all the stimuli and all the faults are compared with typical values for shorts and opens (Table 1). More specifically, all the stimuli are evaluated for each fault; this iteration loop enables specification of test vectors that maximizes the observability of the fault.

Experimental results:

The method according to the invention were applied to a second order band-pass filter as shown in Figure 9, to the fifth order chebychev band-pass filter of Figure 12, and to several other circuits listed in Table 4.

Example 1 (second order band-pass filter of Figure 9):

In the filter of Figure 9, Rg=220kΩ, R1=10Ω, R2=10kΩ, R3=10kΩ, R4=10kΩ, Rd=200kΩ, C1=1.59nf, and C2=1.59nf.

The gradient method has been used for the band-pass filter testing at the circuit's nominal frequency response, 10 kHz. For simplicity, three possible opens and two possible shorts circuits were considered: open Rg, open R2, open R3, short 3&8 and short 6&4. The output voltage was used as a detection mechanism (output parameter) and the detection threshold was set to 5% of the nominal voltage value. In other words, the method of the invention was used to estimate the resistance value R_{fault} beyond which the signature of the output parameter will be modified by more than 5% (Figure 10).

In this example, four out of the five faults have been detected. R_{fault} for open Rg, open R2, and open R3 was lower than $R_{typical}$ and the test vector (10KHz sine wave) was marked as a valid test vector. For short 3&8 R_{fault} was higher than $R_{typical}$ and the test vector was also marked as a valid test vector for this fault. However, for short 6&4, R_{fault} was lower than $R_{typical}$ and the test vector was rejected as a non-valid test vector for this fault.

To validate the efficiency of this method, each fault was reinjected manually into the circuit and simulated. Figure 11 shows the results of the fault simulation over the considered catastrophic defects. In this figure, each fault is analysed to confirm whether or not it was detected at the output node at the 10KHz test frequency. Indeed, all the accepted resistances modified the signature of the fault-free output voltage by more than 5% which has been determined as a detection criteria.

Example 2: Fifth order chebychev filter of Figure 12

The fifth order chebychev filter of Figure 12 has been tested for 25 possible hard faults. The set of stimuli T was selected as the frequency range 0-20kHz. The detection threshold was set to 5% of the nominal output voltage, $R_{typical}$ for open set to 1MΩ, and $R_{typical}$ for shorts set to 1kΩ.

It was found that all the relevant possible shorts and opens are easily detected. The following Table 2 and Table 3 give some possible hard faults, their computed nominal values and the frequency at which they are detected.

Table 2 Fifth order chebychev filter open circuit fault results

OPEN	R_{fault}(ohm)	$R_{typical}$(ohm)	Frequency(Hz)	Decision
R1	1.1K	1Meg	300	Accepted
R2	1.93K	1Meg	300	Accepted
R3	400	1Meg	0	Accepted
R4	662.5	1Meg	0	Accepted
R5	4.83k	1Meg	100	Accepted
R6	2.78k	1Meg	200	Accepted
R7	2.78k	1Meg	200	Accepted
R8	431	1Meg	0	Accepted
R9	555	1Meg	0	Accepted
C1	5.12K	1Meg	100	Accepted
C2	4.43k	1Meg	100	Accepted
C3	2.89k	1Meg	100	Accepted
gm1	872	1Meg	200	Accepted
gm2	243	1Meg	0	Accepted
gm3	1k	1Meg	1k	Accepted

Table 3 Fifth order chebychev filter short circuit fault results

SHORT	R_{fault}(ohm)	$R_{typical}$(ohm)	Frequency(Hz)	Decision
Vin & 0	INF	1k	all frequencies	Accepted
VDD & 0	INF	1k	all frequencies	Accepted
VSS & 0	INF	1k	all frequencies	Accepted
R1 & 0	20 Meg	1k	0	Accepted
R1 & R2	8 Meg	1k	0	Accepted
R5 & R6	85 k	1k	0	Accepted
R9 & 0	50 M	1k	1k	Accepted
in- & 0	25 Meg	1k	0	Accepted
in+ & 0	2e-5	1k	0	Rejected

The obtained fault coverage is 96% with only 5 test vectors (0Hz, 100Hz, 200Hz, 300Hz, 1KHz).

Example 3:

A set of 7 benchmark circuits were simulated. The benchmark circuits ranged from a simple operational amplifier to a complex 8 bit current DAC (digital-to-analog converter). Level 3, Level 28 and level 49 transistor MOSFET models were used in the sensitivity computation environment.

In all experiments the output voltage measurements and/or output current measurements were considered for testing. The detection threshold was set to 6σ where σ is the standard deviation of the fault-free circuit. Table 4 describes the circuit type, the test domain, the number of transistors in the circuit, the number of faults in the fault list obtained through schematic-based fault dictionary, and the total CPU time on a SPARC 10 workstation. The approximated CPU time is given for

serial methods using one simulation per fault. The obtained fault coverage is also provided for comparison purposes.

Table 4 - Benchmark results

Circuit	Test domain	Number of transistors	Number of faults	TestMaxx CPU time(s)	Serial method CPU time(s)*	Fault coverage
Inverter	DC	9	47	0.28	5.68	91.5%
low pass filter	Transient	9	51	0.43	7.92	94.1%
State variable filte	AC	36	184	3.64	334.88	85.3%
Chebychev filter	AD	27	149	5.32	348.16	87.2%
4 bit ADC	DC	153	737	5.46	1341.32	85.7%
8 bit ADC flash	DC	63	295	7.83	256.65	87.4%
8 bit current DAC	Transient	132	669	6.81	1518.63	98.6%

*estimated based on one simulation per fault

The average fault coverage was 90% with small CPU cost. There was no way to compare the fault coverage and the simulation time with other publications due to the large variety of analog benchmarks.

Figure 13 presents the fault coverage as function of the number of test vectors, for an inverter, a low pass filter, a state variable filter, a chebychev filter, a 4-bit analog-to-digital converter, an 8-bit analog-to-digital converter flash, and an 8-bit current digital-to-analog converter.

To summarize, an automatic tool for parallel fault simulation and test vector generation based on a cause-effect approach has been presented. The concept is new, and from our simulation

results, we can conclude that this method is highly efficient. Indeed, fault coverage was as high as 98.6% with simulating time several order of magnitude less than the serial methods.

A plurality of articles have been referred to in the present disclosure. The contents and subject matter of these articles is fully incorporated herein by reference.

Although the present invention has been described hereinabove by way of a preferred embodiment thereof, this embodiment can be modified at will, within the scope of the appended claims, without departing from the spirit and nature of the subject invention.

WHAT IS CLAIMED IS:

1. A method for constructing a fault dictionary for a circuit in view of subsequently testing the circuit, comprising the steps of:

(a) describing the circuit;

(b) extracting a list of faults from the description of the circuit;

(c) in response to the description of the circuit, calculating a fault-free circuit distribution of an output parameter of the circuit;

(d) calculating a faulty circuit distribution of the output parameter in response to the faults of said list;

(e) calculating a fault value from the fault-free and faulty circuit distributions;

(f) storing the calculated fault value in the fault dictionary in view of subsequently specifying at least one test vector for application to the circuit in view of testing said circuit.

2. A method for constructing a fault dictionary as recited in claim 1, in which step (b) comprises extracting from the description of the circuit layout-based faults to form said list.

3. A method for constructing a fault dictionary as recited in claim 1, in which step (b) comprises extracting from the description of the circuit schematic-based faults to form said list.

4. A method for constructing a fault dictionary as recited in claim 1, wherein the circuit comprises a plurality of components and wherein step (c) comprises:

calculating sensitivities of the output parameter to variation of the components of the circuit; and

calculating the fault-free circuit distribution in relation to the calculated sensitivities.

5. A method for constructing a fault dictionary as recited in claim 1, wherein step (d) comprises the steps of:

selecting a stimulus; and

calculating gradients of the output parameter with respect to the faults for the selected stimulus.

6. A method for constructing a fault dictionary as recited in claim 5, further comprising the step of repeating steps (d), (e) and (f) for a plurality of stimuli.

7. A method for constructing a fault dictionary as recited in claim 5, in which step (e) comprises calculating the fault value in relation to the fault-free circuit distribution and the calculated gradients.

8. A method for constructing a fault dictionary as recited in claim 1, wherein the circuit comprises a plurality of components, and wherein:

step (c) comprises calculating sensitivities of the output parameter to variation of the components of the circuit;

step (d) comprises calculating gradients of the output parameter with respect to the faults; and

step (e) comprises calculating the fault value in relation to the calculated sensitivities and gradients.

9. A method for constructing a fault dictionary as recited in claim 1, wherein the fault value is a minimal fault value which, if added to the circuit, causes the output parameter to go out of a predetermined tolerance range.

10. A method for constructing a fault dictionary as recited in claim 8, wherein the fault value is a minimal resistance value which, if added to the circuit, causes the output parameter to go out of a predetermined tolerance range.

11. A method for constructing a fault dictionary as recited in claim 10, wherein the minimal resistance value is given by the relation:

$$R_{f_i} = \frac{6\sqrt{\sum_{i-1}^{N}(S_{x_i}^{out})^2\sigma_{x_i}^2 + \sum_{i\neq j i=i}^{N}\sum_{j=1}^{N} S_{x_i}^{out}\, S_{x_j}^{out}\sigma_{x_{ij}}}}{G_{f_i}^{out}} \qquad (11)$$

where - S_{xi}^{out} is the sensitivity of the output parameter to variations of the circuit component x_i;

- σ_{xi} is a standard deviation of the component x_i;

- S_{xj}^{out} is the sensitivity of the output parameter to variations of the component x_j;

- σ_{xij} is a covariance term; and

- G_{fi}^{out} is the gradient of the output parameter with respect to the fault f_i.

12. A method for constructing a fault dictionary as recited in claim 1, further comprising the steps of:

(g) comparing the fault value calculated in step (e) with a typical fault value;

(h) for each stimulus determining whether each fault is detected or undetected by said stimulus in accordance with the result of said comparison;

(i) building test vectors from the stimuli of said set most susceptible to detect faults in said circuit.

13. A method for building test vectors in view of testing a given circuit, comprising the steps of:

(a) selecting a set of stimuli;

(b) selecting a stimulus of said set;

(c) selecting a fault from a list of faults of said circuit;

(d) from a fault dictionary, finding a fault value related to the selected fault and stimulus;

(e) comparing the faut value found in step (d) to a typical fault value;

(f) determining whether the selected fault is detected or undetected by applying said stimulus to the circuit including the selected fault in accordance with the result of the comparison of step (e);

(g) repeating steps (b), (c), (d), (e) and (f) for each pair of stimulus and fault; and

(h) building test vectors from the stimuli of said set most susceptible to detect faults in said circuit.

14. A method for building test vectors as defined in claim 13, in which, when the fault is an open circuit, step (f) comprises determining that the selected fault is detected by the selected stimulus when the result of the comparison of step (e) is that the fault value found in step (d) is lower than the typical fault value.

15. A method for building test vectors as defined in claim 13, in which, when the fault is a short circuit, step (f) comprises determining that the selected fault is detected by the selected stimulus when the result of the comparison of step (e) is that the fault value found in step (d) is higher than the typical fault value.

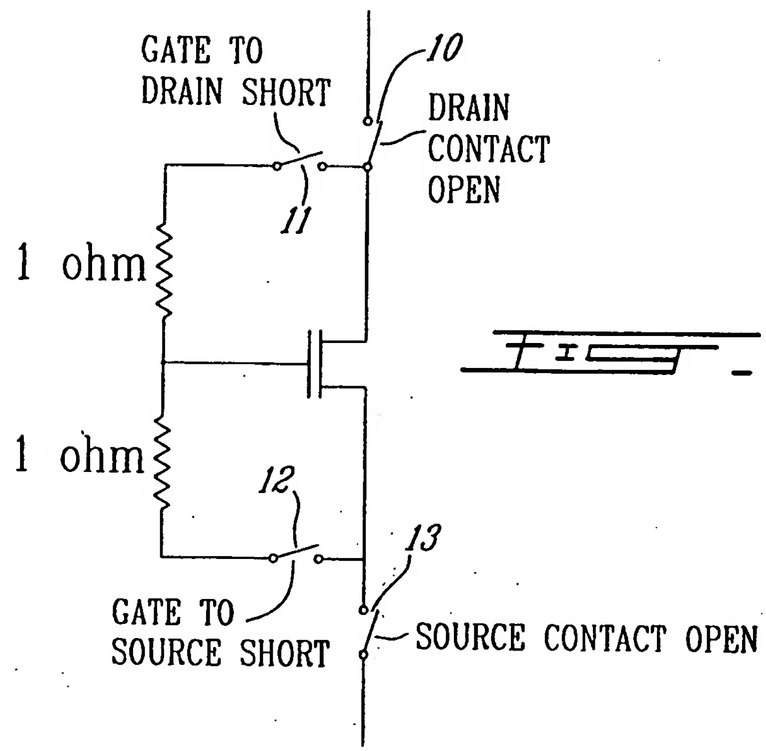


FIG. 1 PRIOR ART

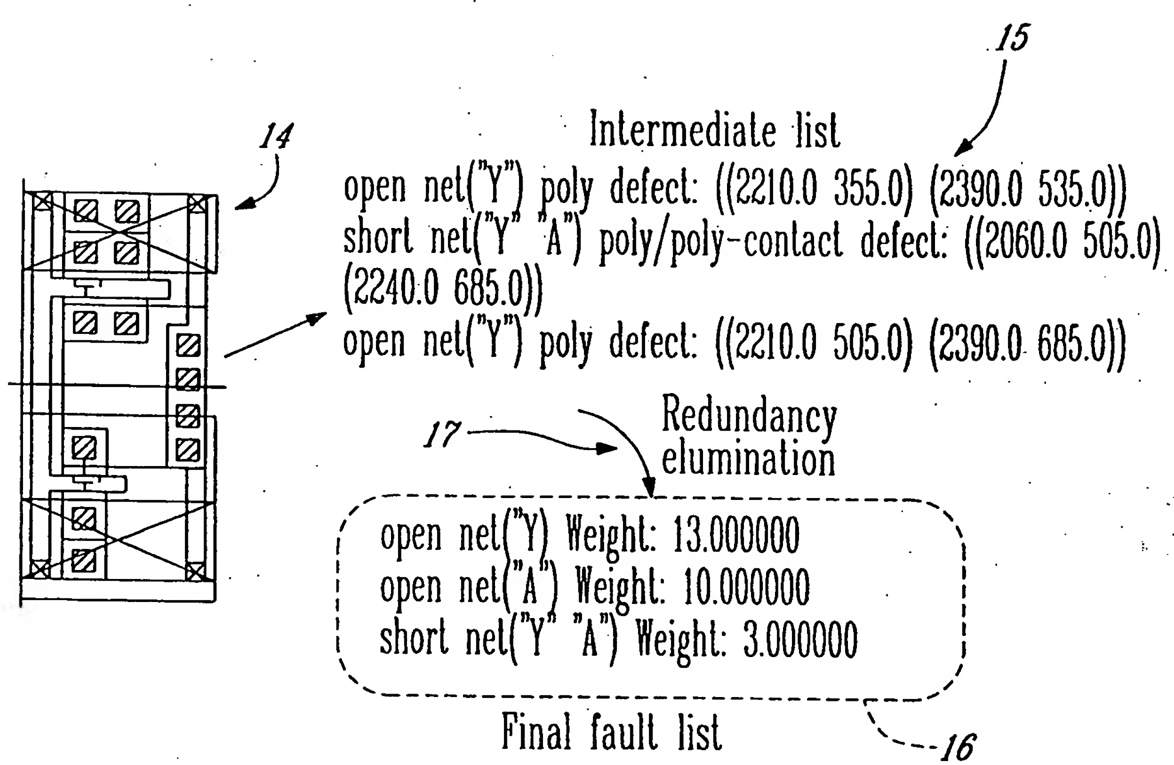


FIG. 2

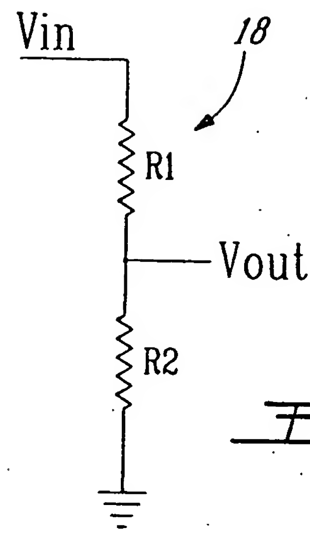


FIG. 3

*voltage divider

Vin in 0 1V

R1 in out 1k

R2 out 0 1K

.end

open in Vin
open 0 Vin
short in 0 Vin
open in R1
open out R1
short in out R1
open out R2
open 0 R2
short out 0 R2
number of listed faults:9
number of redundant faults:3

Undetected fault

Redundant faults

Redundant faults

FIG. 4

open in Vin R1
open 0 Vin R2
short in 0 Vin
open out R1 R2
short in out R1
short out 0 R2

FIG. 5

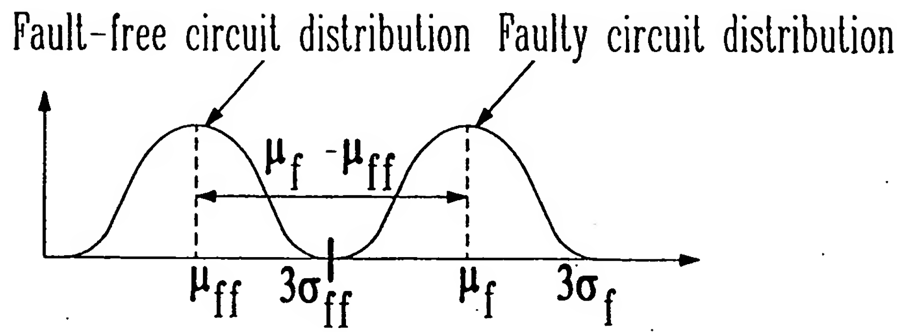

Fault-free circuit distribution
Faulty circuit distribution
$\mu_f - \mu_{ff}$
μ_{ff}
$3\sigma_{ff}$
μ_f
$3\sigma_f$

FIG. 6

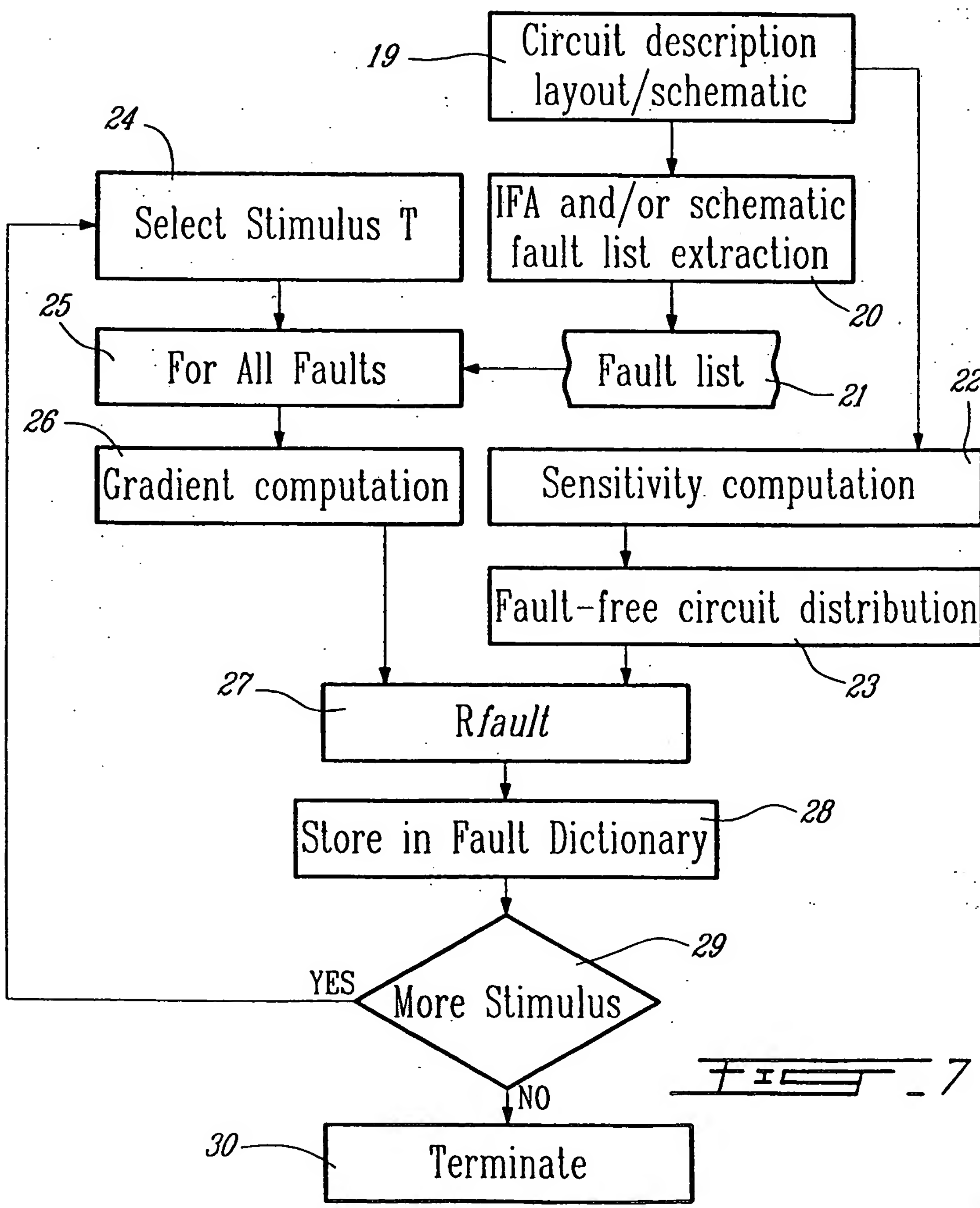
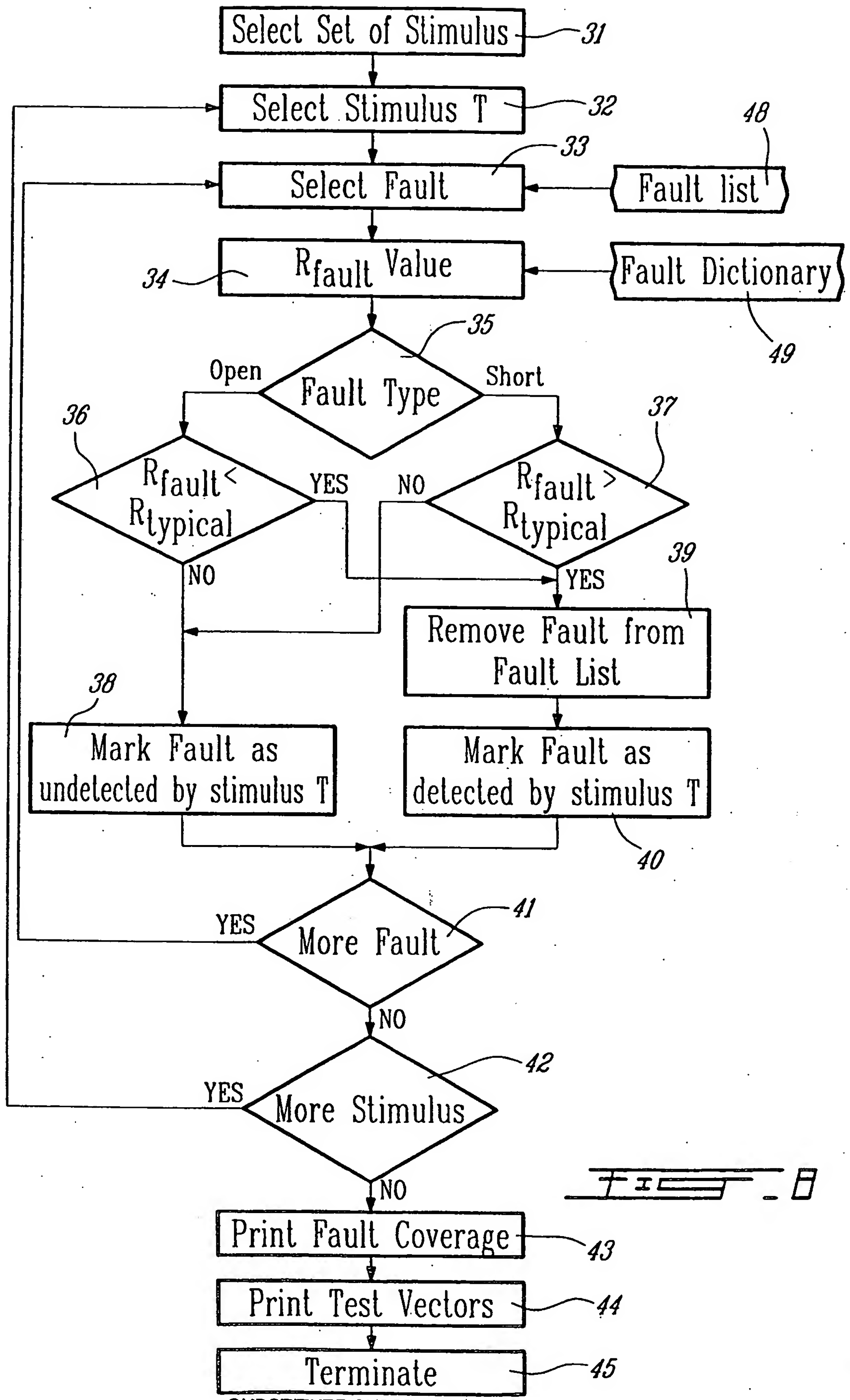

19
Circuit description layout/schematic
24
Select Stimulus T
IFA and/or schematic fault list extraction
20
25
For All Faults
Fault list
21
22
26
Gradient computation
Sensitivity computation
Fault-free circuit distribution
23
27
Rfault
Store in Fault Dictionary
28
29
YES
More Stimulus
NO
30
Terminate

FIG. 7



Select Set of Stimulus
31
Select Stimulus T
32
Select Fault
33
Fault list
48
Rfault Value
34
Fault Dictionary
49
Fault Type
35
Open
Short
Rfault < Rtypical
36
Rfault > Rtypical
37
YES
NO
NO
YES
Remove Fault from Fault List
39
Mark Fault as undetected by stimulus T
38
Mark Fault as detected by stimulus T
40
More Fault
41
YES
NO
More Stimulus
42
YES
NO
Print Fault Coverage
43
Print Test Vectors
44
Terminate
45

FIG. 8

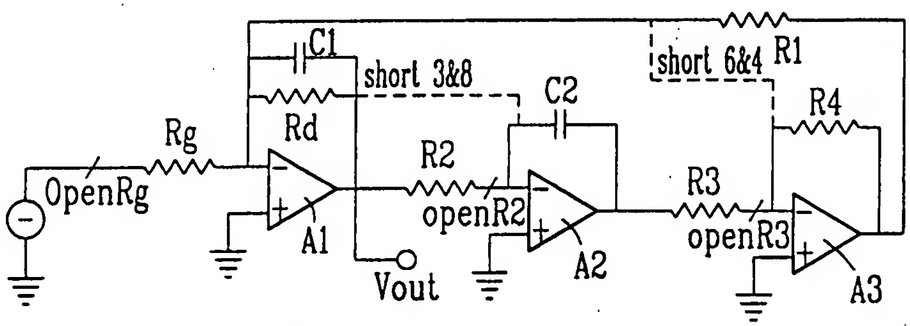


FIG - 9

FIG - 10

TestMaxx

File Options Hard Fault Soft Fault List

Circuit File

/scrgtchd/band_pass.cir Browse...

Log window

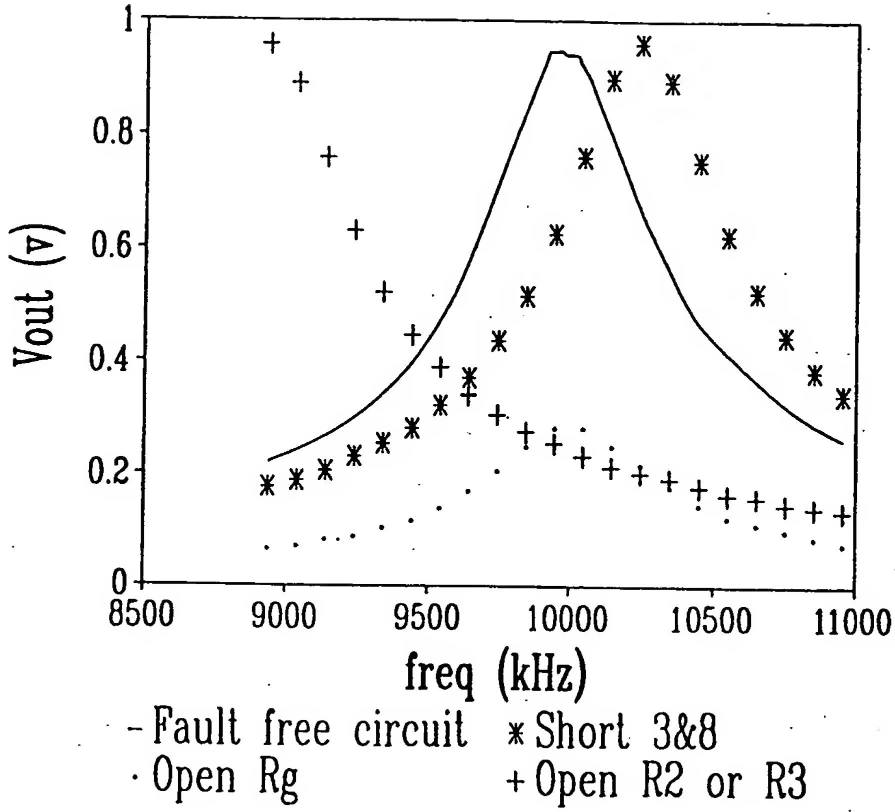
band_pass.heds

* Summary Hard Fault Deterministit Coverage Report

* Circuit: band pass.cir

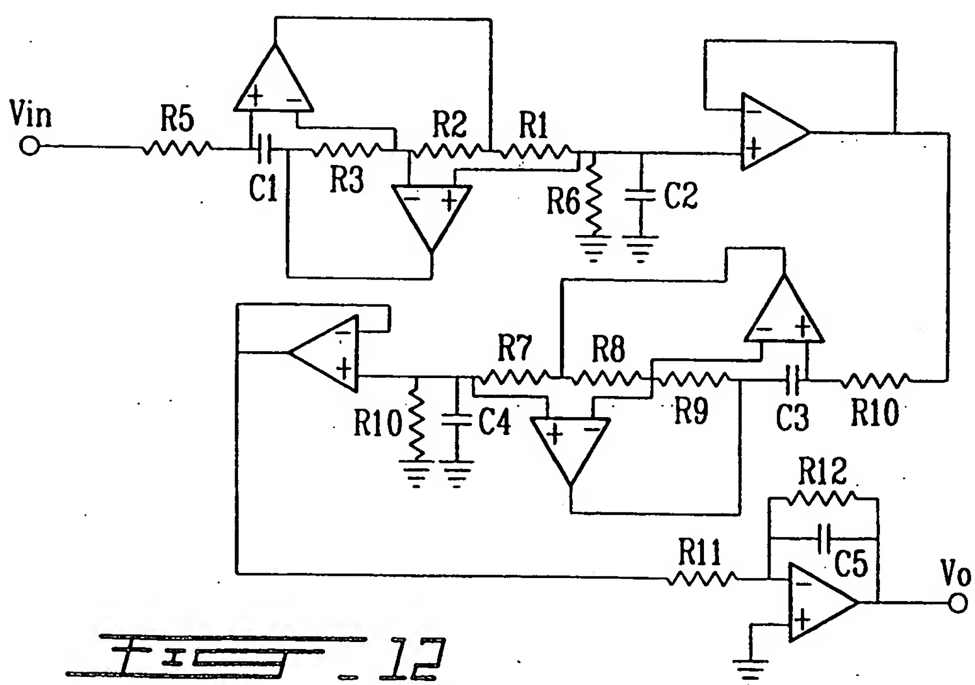
TOTAL FAULT DETECT: 4/5 ---> 0.800000

fault	name	Rfault	Rtypical	test vector	detection status
open.1	Rg	1.003691e+05	1. 000000e+06	1. 000000e+4	X
open.8	R2	5.393087e+03	1. 000000e+06	1. 000000e+4	X
open.6	R3	5.396704e+03	1. 000000e+06	1. 000000e+4	X
short.	3&8	2.034682e+06	1. 000000e+03	1. 000000e+4	X
short.	6&4	2.473909e+01	1. 000000e+03	1. 000000e+4	



Vout (v)
1
0.8
0.6
0.4
0.2
0
8500
9000
9500
10000
10500
11000
freq (kHz)
- Fault free circuit
· Open Rg
* Short 3&8
+ Open R2 or R3

FIG. 11



Vin
R5
C1
R3
R2
R1
R6
C2
R7
R8
R9
C3
R10
R10
C4
R12
C5
R11
Vo

FIG. 12

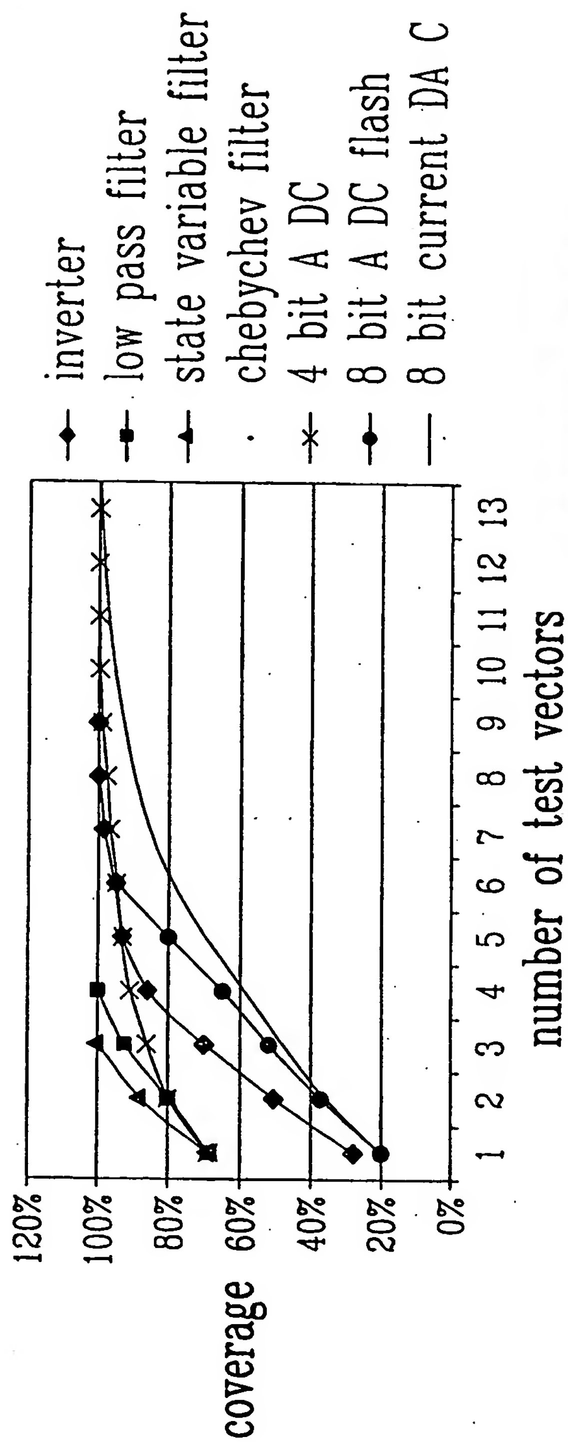

coverage
120%
100%
80%
60%
40%
20%
0%
1 2 3 4 5 6 7 8 9 10 11 12 13
number of test vectors
inverter
low pass filter
state variable filter
chebychev filter
4 bit A DC
8 bit A DC flash
8 bit current DA C

Fig - 13

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 98/00538

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R31/3183 G01R31/316 G01R31/3167

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 228 537 A (HENCKELS ET AL.) 14 October 1980 see column 2, line 41 - column 3, line 23 see column 3, line 61 - column 4, line 63; figures 1-3 see column 5, line 32 - column 6, line 26	1-3,6,12
A	EP 0 568 132 A (SCHLUMBERGER) 3 November 1993 see page 3, line 34 - page 4, line 3; claim 1; figures 1-9	1,13
A	US 5 390 193 A (MILLMAN ET AL.) 14 February 1995 see column 2, line 13 - column 3, line 27; figure 1	1,13

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 1998	21/09/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 98/00538

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 3 649 910 A (VINSANI ET AL.) 14 March 1972 see abstract see column 3, line 25 - line 42 see column 5, line 21 - column 7, line 44; figures 1-3 -----	1,13

1

INTERNATIONAL SEARCH REPORT

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natior pplication No
PCT/CA 98/00538

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